IN THE CLAIMS

Claims 1-56 (Canceled)

57. (New) A method of manufacturing a semiconductor device, comprising the steps of:

(a) mounting a plurality of semiconductor chips on a first surface of a first substrate;

(b) setting the first substrate with the plural semiconductor chips mounted thereon into a mold so that a second surface of the first substrate opposite to the first surface faces a lower mold half of the mold and so that the plural semiconductor chips on the first surface are received into one cavity of the mold;

(c) sealing the plural semiconductor chips with resin in a block to form a seal member while interposing a film between an upper mold half of the mold and the first surface of the first substrate;

(d) releasing the seal member from the mold with use of the film; and

(e) cutting the first substrate and the seal member into individual semiconductor devices,

wherein the first substrate has conductor patterns for wiring which are electrically connecting corresponding

semiconductor chips, and conductor patterns for dummy which are divided from the conductor patterns for wiring, and

wherein, in the sealing step with resin, the film is vacuum-chucked to the upper mold half of the mold.

58. (New) A method of manufacturing a semiconductor device according to claim 57, wherein, in the mounting step, each of the semiconductor chips is arranged over a corresponding conductor pattern for dummy.

59. (New) A method of manufacturing a semiconductor device according to claim 57, wherein, in the sealing step with resin, the second surface of the first substrate is vacuum-chucked to the lower half of the mold.

60. (New) A method of manufacturing a semiconductor device according to claim 57, wherein the first substrate has a first wiring layer exposed on the first surface of the first substrate, the first wiring layer comprises the conductor patterns for wiring and the conductor patterns for dummy, and the conductor patterns for wiring are electrically connected with the semiconductor chips via bonding wires.

61. (New) A method of manufacturing a semiconductor device according to claim 60, wherein the first substrate has an insulating film covering a part of the first wiring layer on the first surface of the first substrate.

62. (New) A method of manufacturing a semiconductor device according to claim 57, wherein the first substrate has a first wiring layer exposed on the second surface of the first substrate, the first wiring layer comprises the conductor patterns for wiring and the conductor patterns for dummy, and further comprising solder bump electrodes formed on the conductor patterns for wiring.

63. (New) A method of manufacturing a semiconductor device according to claim 62, wherein the first substrate has an insulating film covering a part of the first wiring layer on the second surface of the first substrate.

64. (New) A method of manufacturing a semiconductor device according to claim 57, wherein the conductor patterns for dummy includes first conductor patterns for dummy and second conductor patterns for dummy opposing to the first conductor patterns for dummy, each of the first and second

conductor patterns for dummy being divided from the conductor patterns for wiring.

65. (New) A method of manufacturing a semiconductor device, comprising the steps of:

(a) mounting a plurality of semiconductor chips on a first surface of a first substrate;

(b) setting the first substrate with the plural semiconductor chips mounted thereon into a mold so that a second surface of the first substrate opposite to the first surface faces a lower mold half of the mold and so that the plural semiconductor chips on the first surface are received into one cavity of the mold;

(c) sealing the plural semiconductor chips with resin in block to form a seal member while interposing a film between an upper mold half of the mold and the first surface of the first substrate;

(d) releasing the seal member from the mold with use of the film; and

(e) cutting the first substrate and the seal member into individual semiconductor devices,

wherein the first substrate has a plurality of first areas where the semiconductor chips are respectively arranged

thereon, and a second area located around the plurality of first areas,

wherein conductor patterns for wiring are formed in the first areas, and conductor patterns for reinforcing pattern which are divided from the conductor patterns for wiring are formed in the second area of the first substrate, and

wherein, in the sealing step with resin, the film is vacuum-chucked to the upper mold half of the mold.

66. (New) A method of manufacturing a semiconductor device according to claim 65, wherein, in the sealing step with resin, the second surface of the first substrate is vacuum-chucked to the lower half of the mold.

67. (New) A method of manufacturing a semiconductor device according to claim 65, wherein the first substrate has a first wiring layer exposed on the first surface of the first substrate, the first wiring layer comprises the conductor patterns for wiring and the conductor patterns for reinforcing pattern, and the conductor patterns for wiring are electrically connected with the semiconductor chips via bonding wires.

68. (New) A method of manufacturing a semiconductor device according to claim 67, wherein the first substrate has an insulating film covering part of the first wiring layer on the first surface of the first substrate.

69. (New) A method of manufacturing a semiconductor device according to claim 65, wherein the first substrate has a first wiring layer exposed on the second surface of the first substrate, the first wiring layer comprises the conductor patterns for wiring and the conductor patterns for reinforcing pattern, and further comprising solder bump electrodes formed on the conductor patterns for wiring.

70. (New) A method of manufacturing a semiconductor device according to claim 69, wherein the first substrate has an insulating film covering a part of the first wiring layer of the second surface of the first substrate.

71. (New) A method of manufacturing a semiconductor device according to claim 65, wherein the conductor patterns for reinforcing pattern include first conductor patterns for reinforcing pattern and second conductor patterns for reinforcing pattern opposing to the first conductor patterns for reinforcing pattern, each of the first and second

conductor patterns for reinforcing pattern being divided from the conductor patterns for wiring and formed in the second area of the first substrate.